IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Davis et al.

Serial No.: To be assigned

Group Art Unit: To be assigned

Filed: December 11, 2001

Examiner: To be assigned

For: Method and Apparatus for Two Step Memory Write Operations

Attorney Docket No.: 9797-0085-999

December 11, 2001

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This preliminary amendment accompanies the filing of a continuation application. Prior Application No. 09/169,736, filed October 09, 1998, received a notice of allowance on August 13, 2001.

Prior to examination, please amend the above identified application as follows:

IN THE SPECIFICATION:

Marked up versions of all revised paragraphs, showing insertions and deletions, are included in Appendix A.

Change the title of this application to: --Memory System and Method for Two Step Write Operations--.

Insert the following Section Title and paragraph on page, line 1, just after the title:

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of prior U.S. Patent Application Serial No. 09/169,736, filed October 09, 1998, which is incorporated herein in its entirety.

Rewrite the paragraph starting on page 17, line 20, as follows:

As can be seen in Fig. 4, no resource conflicts are observed in the case where a write operation follows another write operation (e.g., write operations 400 and 405). Moreover, data can also be efficiently transferred in the case where a write operation follows a read operation (e.g., read operation 410 and write operation 415). This is because the read data can be followed immediately with write data. Although not illustrated in Fig. 4, the case where a read operation is followed by another read operation also experiences no resource conflicts. These combinations fail to experience such conflicts because the data transfer requested by the given operations are not in contention for the same resources. For example, write data 425 is transferred from data signal lines 114 to column I/O lines 266 before write data 430 needs data signal lines 114. Thus, no resource conflict occurs.

Rewrite the paragraph starting on page 26, line 12, as follows:

The highlighted read operation in Fig. 10 shows the read control being transmitted on control signal lines 112, which causes the memory core to be controlled by signals 710 and 715. The characteristics of memory core 180 affect the time at which the read data is available and delivered via signals 775, which are transmitted from the memory device on data signal lines 114.

IN THE CLAIMS:

Cancel claims 1-37.

Add new claims 38-54 as follows:

38. A memory system, comprising:

a communication channel coupled to a master memory device and coupled to a slave memory device;

the master memory device configured to generate control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device; and

the slave memory device configured to process the read command prior to completing the processing of at least one of the plurality of write commands without causing a column resource conflict at a memory core of the slave memory device.

39. The memory system of claim 38 wherein the slave memory device includes:

a write data buffer to store the associated write information of at least one of the plurality of write commands, the write buffer configured to receive the associated write information in a first step and to retire the associated write information from the write data buffer to the memory core of the slave memory device in a second step.

40. The memory system of claim 39 wherein the master memory device is further configured to generate a first distinct control signal to indicate the transport of the associated write information to the write data buffer in the first step and a second distinct control signal to indicate the retirement of the associated write information to the memory core of the slave memory device in the second step.

41. The memory system of claim 39 wherein the slave memory device is configured to retire the associated write information from the write data buffer to the memory core of the slave memory device when a read command is not being processed at the memory core.

42. The memory system of claim 39 wherein the write data buffer is configured to retire the associated write information in response to any control information other than one associated with processing a read command to the slave memory device.

43. The memory system of claim 39 wherein the write data buffer is configured to retire the write data information in the absence of any control information.

44. The memory system of claim 39 wherein the write data buffer is positioned in the slave memory device.

45. The memory system of claim 39 wherein the write data buffer is positioned in the master memory device.

46. A method of operating a memory system with a master memory device coupled to a slave memory device, the method comprising:

generating with the master memory device control information and associated data information including a plurality of write commands with associated write information for each write command to the slave memory device followed by any operation code other than a read or write command to the slave memory device and then followed by a read command to the slave memory device;

processing the read command at the slave memory device; and

completing the processing of at least one of the plurality of write commands at the slave memory device after processing the read command so as to avoid a column resource conflict at a memory core of the slave memory device.

47. The method of claim 46 further comprising, after the generating step and before the processing step:

transporting the associated write information of at least one of the plurality of write commands into a write data buffer.

48. The method of claim 47 wherein the transporting step is indicated by a distinct transport control signal.

49. The method of claim 47 wherein the completing step further comprises:

retiring the associated write information from the write data buffer to the memory core of the slave memory device wherein the associated write information is retired into the memory core when a read command is not being processed at the memory core.

50. The method of claim 49 wherein the retiring step is indicated by a distinct retire control signal.

51. The method of claim 49 wherein the retiring step is performed in response to any control information other than control information associated with processing of a read command to the slave memory device.

52. The method of claim 49 wherein the retiring step is performed in the absence of any control information.

53. The method of claim 46 wherein the transporting step is performed in the slave memory device.

54. The method of claim 46 wherein the transporting step is performed in the master memory device.

REMARKS

The above amendments delete the originally filed claims in prior application 09/169,736 and add non-elected claims formerly pending in prior application 09/169,736.

No fee is believed to be due with this amendment. However, should the commissioner determine otherwise, he is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 16-1150 (Order No. 009797-0085-999) for any matter in connection with this response, which may be required.

Respectfully submitted,

Date: December 11, 2001

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APPENDIX A

Changes to the Specification

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the time at which the read data is available and delivered via signals 775, which are transmitted from the memory device on data signal lines 114.